ABSTRACT

Circuit structures and associated methods of operation for preventing retrieval of secure information within an integrated circuit by unauthorized use of scan test operation of the integrated circuit. Features and aspects of the invention provide for intercepting scan test related signals within the integrated circuit and for applying an internally generated reset signal to clear any secure information presently loaded into the integrated circuit and stored in flip-flop, register or other memory elements within the integrated circuit. The internally generated reset may be applied prior to entry to scan test to clear any secure information within the integrated circuit at scan test entry. The internally generated reset may also be applied at scan test exit to clear secure information that may be revealed by continued normal operation following scan test operation.